

https://www.synopsys.com/dw/ipdir.php?ds=dwc_ddr_universal_umctl2



Home ▾ / DesignWare IP ▾ / Interface IP ▾ / DDR
/ DesignWare Enhanced Universal DDR Memory Controller (uMCTL2)



DesignWare Enhanced Universal DDR Memory Controller (uMCTL2)

The DesignWare® Enhanced Universal Memory Controller (uMCTL2) is fully configurable controller that allows designers to generate a DDR controller that is optimized for latency, bandwidth, and area. The configurable uMCTL2 allows for the generation of DDR controllers that meet or exceed the requirements of designs ranging from high-performance networking to low-power, cost-sensitive mobile products. The uMCTL2 DDR supports the JEDEC standard DDR4, DDR3, DDR2, LPDDR4, LPDDR3, LPDDR2, and LPDDR/mobile DDR SDRAMs.

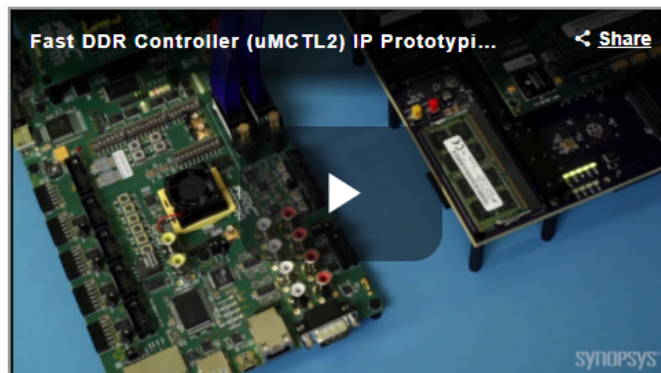
The uMCTL2 delivers maximum bandwidth with low latency. This advanced memory controller accepts memory access requests from between 1 and 16 application-side host ports. Application-side interfaces can be connected to the uMCTL2 either through standard AMBA (AXI4, AXI or AHB) bus interfaces for one or multiple ports, or via Synopsys' custom-defined host-interface H-IF for single-port ultra low latency configurations.

The uMCTL2's low-power features make it useful in power-sensitive designs, and uMCTL2's reliability, availability, and serviceability (RAS) features meet the needs of the most demanding enterprise systems.

The uMCTL2 offers many features to maximize performance: high-priority bypass that reduces latency, configurable look-ahead of up to 64 read and 64 write commands, dual address queues per port to reduce head-of-line blocking, quality of service (QoS) to improve system performance, variable priority commands, a read reorder buffer (RRB) to allow out-of-order execution with in-order responses, and more.

The uMCTL2 supports powerful features to optimize DDR memory efficiency for applications while managing quality of service for individual transaction streams.

- [DesignWare DDR Complete Solution Datasheet](#)
- [DesignWare Enhanced Universal DDR Memory and Protocol Controller IP Datasheet](#)
- [DesignWare IP Prototyping Kits for DDR4/3 and LPDDR4 Controllers](#)



Fast DDR Controller (uMCTL2) IP Prototyping & Integration with DesignWare IP Prototyping Kits

Reduce DDR IP prototyping and integration effort using DesignWare IP Prototyping Kits. The kits provide the essential hardware and software elements needed to start implementing the IP in an SoC in minutes. The included simulation testbench, reference drivers, and application examples enable designers to start their own IP software development right out of the box.

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Highlights Products Downloads and Documentation

- Select a complete multi-ported Enhanced Universal DDR Memory Controller offering 1 to 16 host ports
- Support for JEDEC standard DDR4, DDR3, DDR2, LPDDR4, LPDDR3, LPDDR2, and LPDDR/Mobile DDR SDRAMs
- Compatible with all Synopsys DesignWare DDR PHYs (excluding DDR2/DDR PHYs)
- DFI 4.0, DFI 3.1 or DFI 2.1 compliant interface to DDR PHY

- Boot-time programmable frequency ratio
- Data rates up to 3200 Mbps in 1:2 frequency ratio, using an 800 MHz controller clock and 1600 MHz memory clock (Dependent on process and PHY chosen)
- Data rates up to 1600 Mbps in 1:1 frequency ratio, using an 800 MHz controller clock and 800 MHz memory clock (Dependent on process and PHY chosen)



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